A MONOLITHIC GaAs I.F. AMPLIFIER FOR INTEGRATED RECEIVER APPLICATIONS*

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Abstract

A monolithic GaAs integrated amplifier has been constructed for the 500 to 1000 MHz intermediate frequency band. The amplifier provides 8.0 ± 1.5 dB gain across the band. The output of the amplifier utilizes a source follower configuration to obtain a favorably low output VSWR of less than 1.5:1 (return loss >15 dB). All bias lines with integral bypass capacitors are contained on the chip and this amplifier is suitable for further integration as a building block of a monolithically integrated receiver front end.

Introduction

The development of monolithic microwave integrated circuits (MMICs) for application in integrated receiver front ends requires design, fabrication, and characterization of individual functional monolithic circuits prior to complete integration of the circuitry.[1,2] The components of a receiver front end include a preamplifier, mixer, i.f. amplifier and possibly a local oscillator for pumping the mixer. The configuration of the integrated receiver under development for the 8 GHz satellite communications band consists of a 2-stage FET preamplifier with a minimum gain of 15 dB followed by a FET mixer with a minimum gain of 5 dB in turn followed by an on-chip i.f. amplifier. The total area of this monolithically integrated receiver is anticipated to be about 10 to 15 mm^2. In this paper, we describe the development of a monolithic i.f. amplifier which is intended to be integrated with other circuitry to provide a complete receiver front end function.

The requirements of an i.f. amplifier intended for integration into an MMIC receiver front end are compact circuit size, significant gain, AGC capability, good output match, and sufficiently low noise depending on preamplifier gain. Since the i.f. amplifier is ultimately to be connected to the mixer output through an interstage matching network, no attempt was made to obtain a good noise match or input match to 50 Ω. The amplifier size is kept small through elimination of inductive tuning elements which is possible for this frequency range. Sufficient gain as well as AGC capability are achieved through use of a dual-gate FET in cascode connection as the input transistor. Excellent output matching is achieved using a source follower FET of appropriate dimensions to match 50 Ω output impedance. The following sections describe the design, fabrication, and performance of this monolithic i.f. amplifier.

Circuit Design

The i.f. amplifier was designed to be compact and to contain all biasing circuitry on chip. The compact design was made possible by elimination of inductive matching elements, although it is likely that some form of inductive tuning will be required when the amplifier is interconnected to the mixer output in order to obtain best gain and noise figure. The amplifier was designed using the COMPACT CAD program. The dual-gate FET was modeled using an equivalent circuit composed of single-gate FET equivalent circuits in the common source and common gate connection. A circuit diagram of the i.f. amplifier is shown in Fig. 1.

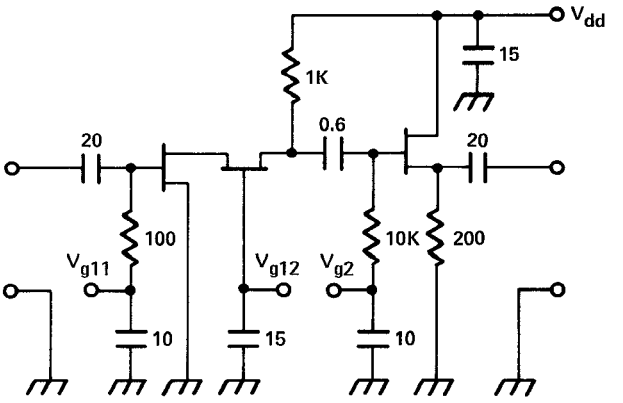

Fig. 1 I. F. Amplifier Schematic Circuit.

Microstrip circuitry on a 0.635 mm thick semi-insulating GaAs substrate is the chosen transmission mode for this amplifier. RF grounding of the active devices is accomplished with top surface ground planes along each edge of the chip. At the IF frequencies, grounding inductance is quite acceptable with this approach. Input and output of the i.f. amplifier are via 50 Ω transmission lines which are isolated by large metal-insulator-metal (MIM) coupling capacitors (10 to 20 pF). Bias lines are provided for each of the FET gates and for V_{dd}. All bias lines are bypassed by large MIM capacitors of 10 to 20 pF value. An interdigital coupling capacitor of value 0.6 pF is used to couple the output of the dual gate FET to the gate of the source follower output stage and simultaneously provide bias isolation. The high impedance at this point permits usage of a relatively small coupling capacitor at low frequencies. However, any parasitic shunt capacitance to the ground plane will have a deleterious effect on amplifier performance.

Since the noise figure of the i.f. amplifier will be reduced by at least 20 dB of gain from the preceding preamplifier and FET mixer, the noise performance was not a primary design concern. The amplifier was designed to provide a nominal gain of 10 dB between 500 and 1000 MHz as shown in Fig. 2. The input match to 50 Ω is required for testing convenience only and is determined by a shunt 100 Ω resistor to ground to

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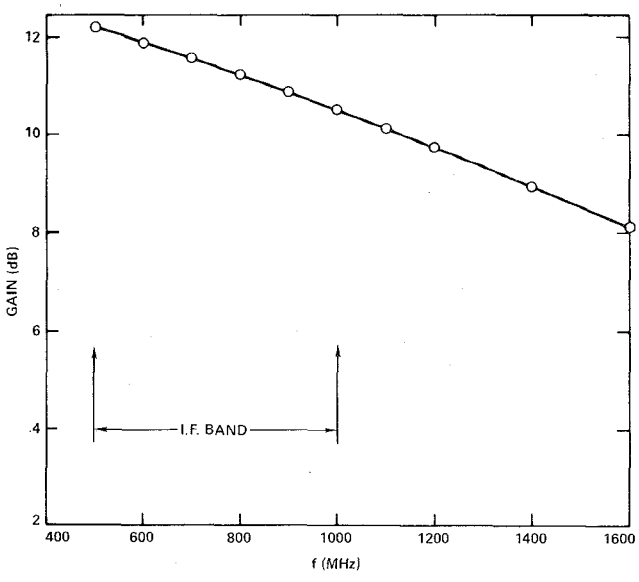

Fig. 2 Calculated gain of I. F. Amplifier.

be about 2:1 VSWR. This resistor will not be necessary in the integrated version of the receiver front end. An excellent output match to 50 Ω is obtained with active matching by using an FET in the common drain connection. In this configuration, the output impedance is approximately equal to the inverse of the FET transconductance. Thus a transconductance of about 20 mS is appropriate for matching to a 50 Ω line. A 200 Ω shunt resistor is used at the output for biasing the source of the output transistor.

Fabrication Technology

The technology for fabrication of MMICs has evolved from GaAs FET technology with many improvements introduced through the use of ion implantation, dry etching, and an all gold metallization system. The basic active device is a 300 μm wide GaAs FET with a 1 μm gate length which has demonstrated high gain and low noise figures and is also well suited for the task of active matching to 50 Ω. Ion implantation directly into semi-insulating GaAs substrates has been selected as the materials technology of choice for fabrication of these circuits due to its simplicity, high reproducibility, and capability of producing nearly planar circuitry.[3] This section will discuss fabrication of MMICs from qualification of the GaAs substrates through chip metallization and separation.

The fabrication technology for ion implanted MMICs begins with the qualification of semi-insulating GaAs substrates for fabrication of ion-implanted FETs. Substrate requirements are basically the maintenance of high resistivity ($\rho > 10^7$ Ω-cm) through the implantation and heat treatments associated with wafer processing.[4] In order to qualify material for use as substrates in MMICs, procedures simulating the process environment have been developed. GaAs ingots are qualified by sampling slices from each end and the middle which are subsequently characterized, subjected to the process simulation procedure, and then recharacterized. Wafers which qualify for the ion implanted MMIC process typically exhibit greater than 10^8 Ω-cm isolation resistance after the 850°C post ion implantation annealing.

Fabrication starts with ion-implantation of the active layer into a qualified substrate. Selenium is used as the n-type dopant and is implanted at an energy of 300 keV and a dose of 3.5×10^{12} cm^{-2} to provide a peak doping of about 1.5 to 1.7×10^{17} cm^{-3} and a pinch-off voltage of about 3.5 V. Definition of active areas may be accomplished by either mesa etching or by selective implantation using a photoresist mask. After implantation, the wafer is capped with silicon nitride and annealed at 850°C for 30 minutes to activate the implant. Fiducial alignment marks are defined on the wafer surface for subsequent realignment capability if selective implantation is used for active layer formation.

Following the ion-implantation and annealing, ohmic contacts are deposited and alloyed for the ohmic contact formation, the FET gates are defined and the first level metallization is delineated. This first level of metal contains the interdigital capacitors, the bottom plates of MIM capacitors, ohmic contact overlays, and interconnecting lines. After first level metallization, the slice is coated with a thick layer of deposited silicon nitride. This nitride is used as the dielectric for the MIM capacitors and as the insulator for crossovers. It also provides a protection layer for the FETs. Via holes are opened in the silicon nitride layer wherever connections to the second level metal are desired. The second level metal is deposited over the nitride layer and plated to a thickness of about 2 to 3 μm to enhance conductivity and minimize transmission losses.

A cross-sectional view of an MMIC chip is shown in Fig. 3. The types of components displayed include interdigital and MIM capacitors, implanted and metal

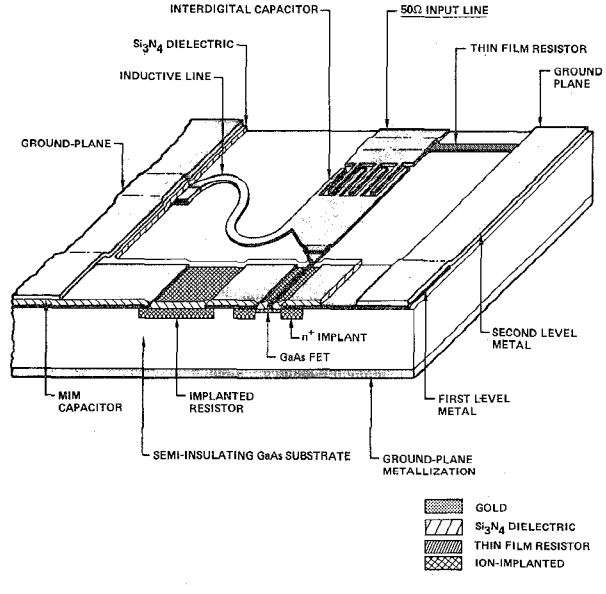

Fig. 3 Cross section of monolithic microwave integrated circuit.

film resistors, distributed inductors, and active FETs. The i.f. amplifier utilizes both interdigital and MIM capacitors, ion-implanted resistors, and GaAs FETs. The MIM capacitors are formed using a silicon nitride dielectric between the first and second levels of metallization. The interdigital capacitors are formed entirely on the first level of metallization and are thus precisely defined by the high-resolution lithography. The ion-implanted resistors are created

using the active layer implant which has a typical sheet resistivity of 1000 ohms per square. Processing of the GaAs FETs occurs simultaneously with that of the passive components.

Completed wafers are coated with a backside metallization to form the microstrip ground plane and aid bondability and are subsequently sawn into individual chips. The i.f. amplifier chips are 2 mm square as seen in the photograph of Fig. 4 which shows an amplifier chip resting on a U.S. dime. The input and output transmission lines can be clearly seen as can the ground planes along either chip edge. The interdigital coupling capacitor may be distinguished between the input and output circuits.

Fig. 4 Photograph of I. F. Amplifier.

Test Results

Completed circuits are mounted into a microstrip test fixture as shown in the photograph of Fig. 5. The circuit is bonded between two alumina microstrip circuits which carry connections for input and output transmission lines and bias leads. In the frequency range of interest, this test fixture has been characterized to have less than 0.2 dB insertion loss with VSWR less than 1.07:1 at input and output (>30 dB return loss). The test fixture is connected to the measurement system using SMA type connectors. Bias is applied at the four screw terminals which are additionally bypassed with 1 μF ceramic capacitors.

The monolithic i.f. amplifier has been characterized for gain, isolation, and input and output match across the band from 500 to 1500 MHz. The measured gain is compared to the predicted gain in Fig. 6. As may be seen from the figure, the measured gain is about 3 dB below the predicted gain at 500 MHz and about 4 dB below the predicted curve at 1000 MHz. The lower gain and increased gain slope can be attributed to parasitic capacitances associated with the relatively large size of the interdigital coupling capacitor which were not included in the initial circuit evaluation. The calculated gain including these additional parasitics is seen to closely predict the observed performance. These parasitics are being minimized through reconfiguration in a second version of this circuit.

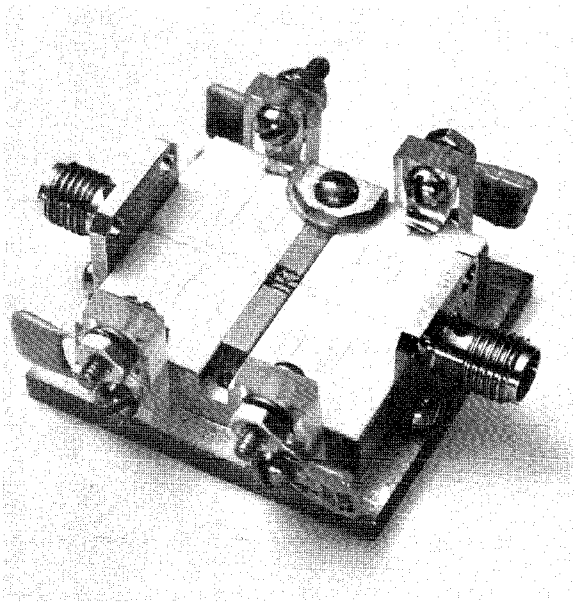

Fig. 5 Photograph of circuit mounted in test fixture.

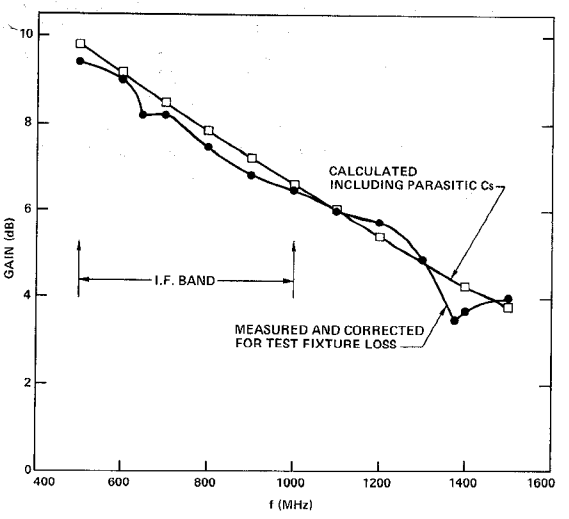

Fig. 6 Measured gain of I. F. Amplifier.

The input and output return loss measured for the i.f. amplifier are shown in Fig. 7. The input VSWR is determined primarily by the 100 Ω shunt resistor and 10 pF bypass and 20 pF isolation capacitors in the input network. The input return loss is about 3 dB smaller than predicted which may be attributed to a reduced value for the bypass capacitor from 10 pF to 7.5 pF in the mask layout. Since, as previously mentioned, the input match is not a primary concern for this amplifier this result is satisfactory. The output match obtained using the source follower configuration is very good across the band from 500 to 1000 MHz as seen in Fig. 7. Output return loss is better than about 15 dB between 800 and 1500 MHz (except at 1100 MHz) dropping to about 10 dB at

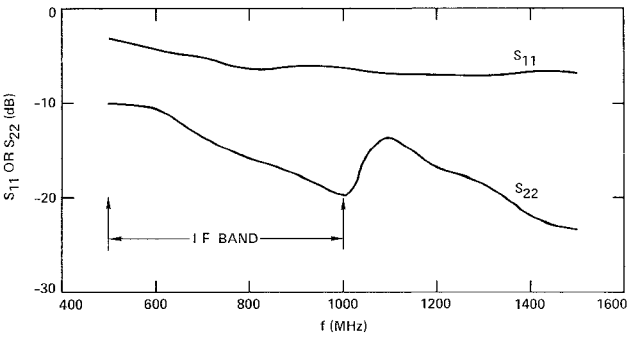

Fig. 7 Measured S_{11} and S_{22} of I. F. Amplifier.

500 MHz. The reduction of output return loss near the low end of the band may again be attributed to somewhat low values of bypass capacitors.

Noise figure of the i.f. amplifier was tested across the 500 to 1000 MHz band. The measured noise figure was 8 dB across the band which, when corrected for the noise of the 100 Ω shunt resistor which will not be present in the final configuration, gives an amplifier noise figure of about 6.25 dB. Noise tuning of the interstage matching could be used to reduce these values when this amplifier is integrated with the mixer circuit. However, such tuning will probably not be necessary since the expected 20 dB gain of the preamplifier and mixer reduce the noise contribution of the i.f. amplifier to less than 0.1 dB at its present performance level.

Conclusions

A monolithically integrated GaAs i.f. amplifier has been built which is suitable for further integration as a building block of a monolithically integrated receiver front end. Bias circuits complete with monolithic MIM bypass capacitors are integrated on this chip. The present chip size of 2 mm square is largely for handling convenience and input/output compatibility with existing test fixtures. In its fully integrated version, this circuit may be reduced to about 1 mm^2 in size.

The gain achieved with the present chip layout is about 8.0 ± 1.5 dB across the band from 500 to 1000 MHz. Reduction of parasitic capacitances is expected to increase the gain and reduce the gain slope by about 2 and 1 dB, respectively. The measured noise performance is consistent with a receiver noise figure governed almost entirely by the performance of preceding preamplifier and FET mixer stages. An excellent output match was obtained using active matching of the source follower configuration to achieve an output return loss of 10 to 20 dB across the band.

References

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